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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,855	03/29/2005	Nicola Da Dalt	10808/172	6363

48581 7590 04/18/2008
BRINKS HOFER GILSON & LIONE/INFINEON
INFINEON
PO BOX 10395
CHICAGO, IL 60610

EXAMINER	
ARENA, ANDREW OWENS	
ART UNIT	**PAPER NUMBER**
2811	
MAIL DATE	**DELIVERY MODE**
04/18/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/511,855	DA DALT, NICOLA	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 January 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Specification

The substitute specification filed 01/08/2008 has been reviewed and accepted.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-21 are rejected under 35 U.S.C. § 102(b) as being anticipated by Ng (US 5,583,359).

RE claim 1, Ng discloses a semiconductor component comprising (Figs 2-4):

a semiconductor substrate (52; col 7 ln 44-46) having an insulating layer (58, 62, 66; col 6 ln 62&65, col 7 ln 2) on the semiconductor substrate surface and having a capacitance structure (50; col 6 ln 52-53) in the insulating layer, wherein the capacitance structure comprises:

a first substructure (top metal layer; 68+75+69 in Fig 1) which has a first cohesive latticed metal region including crossing metal leads (main portion 68 crosses edge portion 69; col 7 ln 4-9) which extends in a first common plane parallel to the substrate surface such that it has common top and bottom surfaces which limit the first cohesive latticed metal region in each of its subregions from above and from below,

wherein the first cohesive latticed metal region is electrically connected to a first connecting line (col 7 ln 21-24, col 8 ln 39-46); and

electrically conductive regions (75; col 7 ln 22-24) electrically isolated from the crossing metal leads (75 isolated by dielectric from 68 & 69; Fig 3) and arranged in openings in the first cohesive latticed metal region of the first substructure at a distance from edge regions of the openings in the first common plane,

wherein the crossing metal leads have a width (width of 69; MPEP § 2111) less than or equal to the distance between the edge regions of the openings and the electrically conductive regions and,

wherein the electrically conductive regions are electrically connected to a second connecting line (col 7 ln 21-24, col 8 ln 39-46), and wherein the electrically conductive regions comprise metal plates (75) between via (74; col 7 ln 21) connections.

RE claim 2, Ng discloses (Fig 2-4) a second substructure (metal layer comprising 65+75+64) parallel to and at a distance from the first substructure wherein the second substructure comprises:

a second cohesive latticed metal region including crossing metal leads (main portion 64 crosses edge portion 65) which extends in a second common plane parallel to the substrate surface such that it has common top and bottom surfaces which limit the second latticed metal region in each of its subregions from above and below; and

electrically conductive regions (e.g., regions of 75),

wherein the first and second substructures are electrically connected by the first and second connecting lines (col 7 ln 21-24, col 8 ln 39-46; also see e.g., Fig 6).

RE claim 3, Ng discloses the second substructure is of substantially the same design as the first substructure, and the first and second substructures are laterally offset from one another such that the electrically conductive regions of the first substructure (uppermost 75) are arranged vertically above crossing points (64 at 65) of the metal leads in the second cohesive latticed metal region of the second substructure, and crossing points of the metal leads in the first cohesive latticed metal region (68 at 69) of the first substructure are arranged vertically above the electrically conductive regions of the second substructure (clear in Fig 2-3, also compare Fig 4A and 4B).

RE claim 4, Ng discloses the crossing points of the metal leads in the first cohesive latticed metal region of the first substructure (68 at 69) are electrically connected to the electrically conductive regions of the second substructure (75) and the electrically conductive regions of the first substructure (uppermost 75) are electrically connected to the crossing points of the metal leads in the second cohesive latticed metal region of the second substructure (64 at 65) by means of at least one respective via connection (col 7 ln 21 and col 8 ln 39-46).

RE claim 5, Ng discloses the second cohesive latticed metal region of the second substructure is laterally offset from the first substructure, so that the electrically conductive regions of the first substructure (uppermost 75) are arranged vertically above the crossing points of the metal leads in the second cohesive latticed metal region of the second substructure (64 at 65).

RE claim 6, Ng discloses the electrically conductive regions of the first substructure (uppermost 75) and the crossing points of the metal leads in the second

cohesive latticed metal region of the second substructure (64 at 65) are electrically connected by means of one or more respective via connections (74; col 7 ln 21).

RE claim 7, Ng discloses a metal plate (60; col 8 ln 60) electrically connected to one of the crossing points of the metal leads in a the cohesive latticed metal region of the first substructure (68 at 69) and to the electrically conductive regions of the second substructure (75) by means of one or more respective via connections (72, 74).

RE claim 8, Ng discloses the first cohesive latticed metal region has at least two square or round openings (e.g., one on either side of 75).

RE claim 9 Ng discloses the first and second connecting lines are at different electrical potentials (col 7 ln 21-24, col 8 ln 39-46; also see e.g., Fig 6).

Re claim 10, Ng discloses a first non-parasitic capacitance exists between the crossing metal leads of the cohesive latticed metal region and the electrically conductive regions of the first substructure and a second non-parasitic capacitance exists between the first and second connecting lines, and wherein the magnitude of the first non-parasitic capacitance differs from the magnitude of the second non-parasitic capacitance (inherent in structure - see MPEP § 2112.01).

RE claim 11, Ng discloses a semiconductor component having an integrated capacitance structure, the component comprising (Figs 2-4):

a semiconductor substrate (52; col 7 ln 44-46) having a surface;

an insulating layer (58, 62, 66; col 6 ln 62&65, col 7 ln 2) overlying the surface of the semiconductor substrate;

a capacitance structure (50; col 6 ln 52-53) in the insulating layer, wherein the capacitance structure comprises:

a first metal lattice including intersecting metal leads (main portion 68 crosses edge portion 69; col 7 ln 4-9) in a first common plane parallel to the substrate surface;

a second metal lattice including intersecting metal leads (main portion 64 crosses edge 65; col 7 ln 4-9) in a second common plane parallel to the substrate surface;

electrically conductive regions (75; col 7 ln 22-24) arranged in openings in the first and second metal lattices and electrically isolated from the intersecting metal leads (75 isolated by dielectric from 68 & 69; Fig 3), the electrically conductive regions spaced apart from edge regions of the openings by the insulation layer,

wherein the intersecting metal leads have a width (width of 69; MPEP § 2111) less than or equal to the distance between the edge regions of the openings and the electrically conductive regions; and

wherein the first and second metal lattices are laterally offset from one another, such that the electrically conductive regions of the first metal lattice (uppermost 75) are substantially vertically above crossing points of the second metal lattice (64 at 65), and crossing points of the first metal lattice (68 at 69) are substantially vertically above the electrically conductive regions of the second metal lattice (75); and

first and second electrical connections between the first and second lattices such that the first and second electrical connections are at different electrical potential (inherent in connection to different polarities: col 7 ln 21-24, col 8 ln 39-46).

RE claim 12, Ng discloses the electrically conductive regions (75) comprise metal plates (col 8 ln 60) or node points (reads on anything per MPEP § 2111).

RE claim 13, Ng discloses the electrical connections comprise:

first connecting lines (70, 72, 74 on right in Fig 3; col 7 ln 21-24) electrically connecting the electrically conductive regions of the first metal lattice (uppermost 75) to crossing points of the second metal lattice (64 at 65); and

second connecting lines (70, 72, 74 on left in Fig 3) electrically connecting crossing points of the first metal lattice (68 at 69) to the electrically conductive regions of the second metal lattice (75).

RE claim 14, Ng discloses a metal plate (60; col 8 ln 60) in a third common plane parallel to the substrate surface and electrically coupled to the first and second metal lattices by the first and second electrical connections.

RE claim 15, Ng discloses a third metal lattice including intersecting metal leads (main portion 60 crosses edge 61; col 7 ln 4-9) in a third common plane parallel to the substrate surface, wherein the intersecting metal leads define openings (on either side of 75), wherein the openings are devoid of electrically conductive regions, and wherein the intersecting metal leads are electrically connected to the first and second metal lattices by the electrical connections (72, 74).

RE claim 16, Ng discloses a semiconductor component having an integrated capacitance structure (50; col 6 ln 52-53), the component comprising (Figs 2-4):

an insulating layer (58, 62, 66; col 6 ln 62&65, col 7 ln 2);

a first metal lattice including intersecting metal leads (main portion 68 crosses edge portion 69; col 7 ln 4-9) in a first common plane;

a second metal lattice including intersecting metal leads (main portion 64 crosses edge 65; col 7 ln 4-9) in a second common plane;

electrically conductive regions (75; col 7 ln 22-24) electrically isolated from the crossing metal leads (75 isolated by dielectric from 68 & 69; Fig 3) and arranged in openings in at least one of the first and second metal lattices, the electrically conductive regions spaced apart from edge regions of the openings by the insulation layer,

wherein the intersecting metal leads have a width (width of 69; MPEP § 2111) less than or equal to the distance between the edge regions of the openings and the electrically conductive regions; and

wherein the first and second metal lattices are laterally offset from one another, such that the electrically conductive regions of the first metal lattice (uppermost 75) are substantially vertically above crossing points of the second metal lattice (64 at 65), and crossing points of the first metal lattice (68 at 69) are substantially vertically above the electrically conductive regions of the second metal lattice (75);

a third metal structure (60; col 8 ln 60) in the insulating layer in a third common plane the third metal structure comprising one of a third metal lattice or a metal plate; and

first and second electrical connections between the first and second lattices such that the first and second electrical connections are at different electrical potential (inherent in connection to different polarities: col 7 ln 21-24, col 8 ln 39-46).

RE claim 17, Ng discloses the third metal structure comprises a metal plate (60) electrically coupled to the electrically conductive regions (75) of the first and second metal lattices by the first and second electrical connections (72, 74; col 7 ln 21-24).

RE claim 18, Ng discloses the third metal structure comprises a third metal lattice including intersecting metal leads (main portion 60 crosses edge 61; col 7 ln 4-9), wherein the intersecting metal leads define openings (either side of 75), wherein the openings are devoid of electrically conductive regions, and wherein the intersecting metal leads are electrically connected to the electrically conductive regions of the first and second metal lattices by the first and second electrical connections (col 7 ln 21-24).

RE claim 19, Ng discloses the first electrical connection (74 on right in Fig 3) electrically connect the electrically conductive regions of the first metal lattice (75) to the crossing points of the second metal lattice (64 at 65), and

wherein the second electrical connection (74 on left in Fig 3) electrically connect the crossing points of the first metal lattice (68 at 69) to the electrically conductive regions of the second metal lattice (75).

RE claim 20, Ng discloses the third metal structure comprises a third metal lattice including intersecting metal leads (60 crosses 61) and electrically conductive regions (75) in openings defined by the intersecting metal leads.

RE claim 21, Ng discloses non-parasitic capacitances exist between the electrically conductive regions and intersecting metal leads in the first, second, and third metal lattices and wherein non-parasitic capacitances exist between the first and second connecting lines (inherent in structure - see MPEP § 2112.01).

Response to Arguments

Applicant's arguments filed 01/08/2008 have been fully considered but they are not persuasive.

It is not clear from the arguments against the 102 rejection (pg 12-14) exactly what features that are recited in the claims are alleged not to be present in Ng. As seen in Fig 3 of Ng, the capacitor includes several substructures (layer of 58, layer of 62, etc) which each include a latticed region (56+57, 60+61, etc) and conductive regions (75) that are electrically isolated from the latticed region. Ng discloses "a width" as claimed.

The following comments are presented in the interest of compact prosecution. The claim language: "vertically above" does not require vertical alignment; "openings" does not require distinct openings; "lattice" is very broad. See MPEP § 2111.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kuroda (US 6,327,134) is very similar to applicant's claimed invention and differs only in not disclosing the capacitor is in an insulating layer on a semiconductor substrate. However the claim language "has a width..." encompasses Kuroda since it does not exclude that the width is greater than the claimed distance. Kuroda could be used in combination with Ng to arrive at applicant's disclosed invention.

Baker (US 6,410,955) is evidence that the relationship between the claimed width and distance is a recognized result effective variable (e.g., Fig 2; col 4 ln 59-64).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571)272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571- 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. For information of PAIR system, see http://pair-direct.uspto.gov. For questions on access to Private PAIR, call 866-217-9197 (toll-free). For assistance or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andrew O. Arena/
Examiner, Art Unit 2811
11 April 2008

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811